



DISCIPLINE ACADEMIC SHEET
ACADEMIC YEAR 2025 – 2026

1. PROGRAMME DATA

1.1. Higher Education Institution	UNIVERSITY OF CRAIOVA
1.2. Faculty	Automation, Computers and Electronics
1.3. Department	Computers and Information Technology
1.4. Field of Study	Computers and Information Technology
1.5. Study level	L(License / Undergraduate)
1.6. Organizational form	IF
1.7. Study Program (name/code) /Qualification	Computers / L2060101010

2. DISCIPLINE DATA

2.1 Discipline Name				Computer Structure and Organization			
2.2 Course Activities Holder				Dumitrașcu Eugen			
2.3. Practical Activities Holder				Popescu Horațiu-Samir			
2.4. Study Year	2	2.5. Semester	2	2.6. Evaluation type	E	2.7. Discipline regime	DOB

3. ESTIMATED TOTAL TIME (hours per semester of teaching activities)

3.1. Number of hours per week	5	in which: 3.2 course	2	3.3. sem./lab./pr.	1/2/0
3.4. Total hours of curriculum	70	in which: 3.5 course	28	3.6. sem./lab./pr.	14/28/0
3.7. Time distribution - hours/week					hours
Study after manual, course support, bibliography and notes					28
Additional documentation in library, on specialized electronic platforms and field					9
Training seminars / labs, homework, portfolios and essays					14
Tutorial					0
Examinations					2
Other activities.....					2
Total hours per individual activities					55
3.8. Total hours per semester					125
3.9. Number of credits					5

4. PRECONDITIONS (where appropriate)

4.1. of curriculum	• Logical Design I, Logical Design II, Computer Systems Architecture
4.2. of competence	• Digital Design using combinational logic schemes; VHDL modeling and synthesis

5. CONDITIONS (where appropriate)

5.1. of the course	The course is presented in a Power Point presentation, using video projector from course room and the examples are presented on the blackboard.
5.2. of seminar/ laboratory/project	- The laboratory is taken in the laboratory rooms for Hardware destination. - The lab work is done in VHDL and Xilinx with Modelsim.

6. COURSE OBJECTIVES – expected learning outcomes that are supported by completing and passing the course

Knowledge	Student/Graduate: - Describes, identifies, summarizes elementary concepts and methods in the structure and organization of computing systems. - Identify the MIPS architecture of RISC processors. - Study the assembly language for RISC processors with the MIPS architecture
Skills (Abilities)	Student/Graduate: - Develops models for various components of computing systems, hardware and software, and evaluates functional and non-functional characteristics. - Uses specific methods and tools for the analysis, design and implementation of computing systems. - Develops hardware models for various components of computing systems
Responsibility and autonomy	Student/Graduate: - Carry out processes in the design of digital systems, taking on different roles in the team and describing the results clearly and concisely, verbally and in writing. - Apply the ethical and deontological values of the engineering profession, practice logical reasoning, evaluation and self-evaluation in decision-making. - Have an honorable, responsible, ethical behavior, in the spirit of the law to ensure the reputation of the profession.

7. CONTENT

7.1. Course	The method of implementation	Teaching methods	Allocated time (hours)
1. Signed Number Representation in Computers	face to face	Lecture presentation using Power Point.	2
2. Addition of Unsigned Binary Numbers	face to face	Lecture presentation using Power Point.	2
3. Addition and Subtraction of Signed Binary Numbers	face to face	Lecture presentation using Power Point.	4
4. Computer Organization - Fundamental Concepts	face to face	Lecture presentation using Power Point.	4
5. Architecture and Organization of MIPS Processor	face to face	Lecture presentation using Power Point.	4
6. Simplified Structure of a MIPS Processor	face to face	Lecture presentation using Power Point.	4
7. Pipeline Structure of a MIPS Processor	face to face	Lecture presentation using Power Point.	4
8. Memory Hierarchy	face to face	Lecture presentation using Power Point.	4

Bibliography:
1. Ionescu Augustin-Iulian – <i>Noțiuni de aritmetică a calculatoarelor</i> , course notes
2. Ionescu Augustin-Iulian – <i>Structura și organizarea calculatoarelor</i> , course notes
3. Patterson David, Hennessy John – <i>Computer Organization and Design</i> , Morgan Kaufmann Publishers, 2004
4. David A. Patterson, John L. Hennessy – <i>Organizarea și proiectarea calculatoarelor</i> – ALL EDUCATIONAL, Bucuresti, 2002
5. David A. Patterson, John L. Hennessy – <i>Computer Organization and Design MIPS Edition</i> – 6th Edition, Elsevier Science & Technology, 2020
6. David A. Patterson, John L. Hennessy – <i>Computer Organization and Design The Hardware-Software Interface</i> – 5th, Elsevier Science & Technology, 2013
7. Cernian Oleg – <i>Computer Architecture</i> , Editura Sitech, Craiova, 2005
8. Cernian Oleg – <i>Computer organisation</i> – Course support, Editura Sitech, Craiova, 2005
9. Andrew S. Tanenbaum - <i>Structured Computer Organization</i> – Fourth Edition, Prentice-Hall, Inc. 2001
10. Mostafa Abd-El-Barr, Hesham El-Rewini – <i>Fundamentals of Computer Organization and Architecture</i> – John Wiley & Sons, 2005
11. Hesham El-Rewini, Mostafa Abd-El-Barr – <i>Advanced Computer Architecture and Parallel Processing</i> - John Wiley & Sons, 2005

7.2. Seminar/laboratory/project	The method of implementation	Teaching methods	Allocated time (hours)
<i>Seminar</i>			
1. Signed Number Representation	face to face	Presentation and solution of problems related computer arithmetic	2
2. Addition and Subtraction of Signed Binary Numbers	face to face	Presentation and solution of problems related computer arithmetic	2
3. MIPS Assembly languages	face to face	Presentation of programs written in Assembly Languages for MIPS	4
4. Pipeline of MIPS	face to face	Presentation and solution of data hazard in pipeline	4
5. Memory Hierarchy	face to face	Presentation and solution of problems related cache memory	2
<i>Laboratory</i>			
1. What a FPGA is?	face to face	FPGA and Spartan 3 board presentation	2
2. One-bit adder with logical gates	face to face	Implementing and simulating the schemes using XILINX ISE 9.2i, ModelSim on Spartan 3 board.	2
3. Four-bit adder with logical gates	face to face	Implementing and simulating the schemes using XILINX ISE 9.2i, ModelSim on Spartan 3 board.	2
4. Four-bit adder/subtractor with logical gates	face to face	Implementing and simulating the schemes using XILINX ISE 9.2i, ModelSim on Spartan 3 board.	2

5. Four-bit adder/subtractor in VHDL	face to face	Implementing and simulating the schemes using XILINX ISE 9.2i, ModelSim on Spartan 3 board.	2
6. MIPS Implementation - PC + ROM	face to face	Implementing and simulating the schemes using XILINX ISE 9.2i, ModelSim on Spartan 3 board.	4
7. MIPS Implementation - complete	face to face	Implementing and simulating the schemes using XILINX ISE 9.2i, ModelSim on Spartan 3 board.	4
8. MIPS Simulation	face to face	Implementing and simulating the schemes using XILINX ISE 9.2i, ModelSim on Spartan 3 board.	4
9. MIPS - BEQ instruction	face to face	Implementing and simulating the schemes using XILINX ISE 9.2i, ModelSim on Spartan 3 board.	2
10. MIPS - Assembly Programming using MARS	face to face	Implementing and simulating the schemes using XILINX ISE 9.2i, ModelSim on Spartan 3 board.	2
11. Laboratory sessions recoveries.	face to face		2
Bibliography:			
1. David A. Patterson, John L. Hennessy – <i>Computer Organization and Design MIPS Edition</i> – 6th Edition, Elsevier Science & Technology, 2020			
2. David A. Patterson, John L. Hennessy – <i>Computer Organization and Design The Hardware-Software Interface</i> – 5th, Elsevier Science & Technology, 2013			

8. Correlating the content of the discipline with the expectations of representatives from the epistemic community, professional associations and representative employers in the field related to the program

The content of the Computer Structure and Organization course is aligned with the current expectations of the academic and professional community in the fields of computer engineering and information technology.

It develops the students' ability to understand and analyze the internal structure and operation of computer systems, including the organization and pipeline structure of processors such as MIPS. These competencies are consistent with the requirements of employers in areas such as hardware design, embedded systems development, computer architecture analysis, and low-level software engineering, where a solid understanding of hardware–software interaction is essential.

Through its theoretical and practical components, the course contributes to the formation of professional skills required for the design, optimization, and evaluation of modern computing systems.

9. EVALUATION

Activity Type	9.1. Evaluation criteria	9.2. Evaluation methods	9.3. Final mark weight
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9.4. Course	Correctly solving three problems	Written paper exam Periodic quizzes at course	70% 10% bonus (maximum 1 point on final grade)
9.5. Seminar/laboratory/project	S: Solving problems given as homework	Homework evaluation	10%
	L: Laboratory sessions	Grading during lab work and homework	20%
9.6. Minimum standard of performance			
The mark of the written exam must be at least 5 and will have 70% weight from final mark. The average obtained in the seminar homework will have a weight of 10% of the final grade. The average of marks obtained in the laboratory sessions must be at least 5 (minimum task completion for all laboratory works and homework) will have 20% weight from the final mark. Bonus from course will be maximum 1 point to the final grade before rounding. Minimum passing grade obtained by the weighted average is 5.			

Date of Completion	Signature of the Course Activities Holder,	Signature of the Practical Activities Holder,
23.08.2025		

Date of Approval in the Department	Signature of the Department Director,
25.08.2025	Ș.I.dr.ing. Nicolae ENESCU

Date of Approval in the Faculty	Signature of the Dean,
	Prof.dr.ing. Dorin ȘENDRESCU