

CONTENTS

| | | | |
|---|------------|--|------|
| Preface | v | | |
| Chapter 1 Negative Numbers Representation | 1-1 | | |
| 1. Complement and its calculation | 1-1 | | |
| 1.1. Concept of complement | 1-1 | | |
| 1.2. Methods for complement calculation | 1-3 | | |
| 1.2.1. Radix 10 | 1-3 | | |
| 1. 10's complement | 1-3 | | |
| 2. 9's complement | 1-4 | | |
| 1.2.2. Radix 2 | 1-6 | | |
| 1. 2's complement | 1-6 | | |
| 2. 1's complement | 1-7 | | |
| 2. Special Codes for negative numbers representation | 1-8 | | |
| 2.1. General formulation of the problem | 1-8 | | |
| 2.2. Sign – Magnitude representation | 1-10 | | |
| 2.3. Two's Complement representation | 1-12 | | |
| 2.3.1. General considerations | 1-12 | | |
| 2.3.2. Variant 1 | 1-12 | | |
| 2.3.3. Variant 2 | 1-16 | | |
| 2.3.4. Variant 3 | 1-17 | | |
| 2.4. One's Complement representation | 1-20 | | |
| 2.4.1. General considerations | 1-20 | | |
| 2.4.2. Variant 1 | 1-20 | | |
| 2.4.3. Variant 2 | 1-24 | | |
| 2.4.4. Variant 3 | 1-27 | | |
| 2.5. Shifting of signed binary numbers | 1-30 | | |
| Chapter 2 Forms of Information Representation in Digital Computers | 2-1 | | |
| 1. General considerations | 2-1 | | |
| 2. Fixed - Point representation of numbers | 2-3 | | |
| 2.1. Introductory concepts | 2-3 | | |
| 2.2. Analysis of the representation ranges | | | |
| | | for positive fractional numbers | 2-4 |
| | | 2.3. Analysis of the representation ranges for negative fractional numbers | 2-5 |
| | | 3. Floating Point representation of numbers | 2-13 |
| | | 3.1. General considerations | 2-13 |
| | | 3.2. FLP formats | 2-14 |
| | | 3.3. Representation ranges for binary FLP numbers | 2-18 |
| | | 3.4. Total number of expressible numbers | 2-23 |
| | | 3.5. FLP representation and real number system | 2-25 |
| | | 3.6. Example of FLP representation | 2-26 |
| | | 3.7. Power of 2 radix FLP representation | 2-28 |
| | | 3.8. Example of FLP representation in base 16 | 2-30 |
| | | 3.9. Comparative analysis of representation errors | 2-32 |
| | | 3.10. Example of FLP representations in different computer families | 2-34 |
| | | 3.10.1. Felix C family | 2-34 |
| | | 3.10.2. PDP-11 family | 2-45 |
| | | 3.11. IEEE Floating Point Standard 754 - 85 | 2-51 |
| | | 3.11.1. Short history | 2-51 |
| | | 3.11.2. Basic FLP formats | 2-51 |
| | | 3.11.3. Normalized Numbers | 2-54 |
| | | 3.11.4. Examples of normalized number representations | 2-58 |
| | | 3.11.5. Denormalized numbers | 2-60 |
| | | 3.11.6. Representation of number 0 | 2-65 |
| | | 3.11.7. Representation of infinity | 2-67 |
| | | 3.11.8. Not a Number (NaN) representation | 2-69 |
| | | 3.11.9. Recapitulation of all IEEE FLP Standard 754 – 85 numerical types | 2-70 |
| | | 3.11.10. IEEE FLP Standard 754 – 85 representation on real axis | 2-71 |
| | | 4. Representation of alphanumeric information | 2-75 |
| | | 4.1. Introduction | 2-75 |
| | | 4.2. Conditions for alphanumeric character code | 2-75 |
| | | 4.3. ASCII - 8 and EBCDIC codes | 2-77 |
| | | 4.3.1. ASCII alphanumeric code | 2-77 |

| | |
|--|------------|
| 4.3.2. EBCDIC alphanumeric code | 2-79 |
| 4.4. Alphanumeric information | 2-81 |
| 4.5. Unicode character set | 2-81 |
| 5. Decimal information representation | 2-83 |
| Chapter 3 General organisation of a digital computer. The von Neumann's model. Instruction Cycle | 3-1 |
| 1. Definition of a digital computer. Computer architecture, computer organisation, computer implementation | 3-1 |
| 2. Short history on stored program computers concept | 3-4 |
| 3. The von Neumann's principles | 3-7 |
| 4. The von Neumann's model of a digital computer | 3-12 |
| 5. Instruction cycle | 3-24 |
| 5.1. Principle of the Digital Computer Operation | 3-24 |
| 5.2. Implementation of the Instruction Cycle | 3-25 |
| Chapter 4 Central Processing Unit | 4-1 |
| 1. CPU organisation and operation flowchart | 4-1 |
| 1.1. General concepts | 4-1 |
| 1.2. Flowchart of CPU operation | 4-3 |
| 1.3. General structure of a CPU | 4-5 |
| 1.4. The evolution of CPU during the FETCH Phase | 4-8 |
| 1.5. The evolution of CPU during the EXECUTE Phase | 4-9 |
| 2. Techniques for balancing the speeds of CPU and main memory | 4-11 |
| 2.1. General considerations | 4-11 |
| 2.2. Widening the memory bus | 4-12 |
| 2.3. Increasing the number of levels in the memory hierarchy | 4-16 |
| 2.4. Prefetching | 4-18 |
| 3. An example of CPU with general registers set organisation | 4-20 |

| | |
|---|------------|
| Chapter 5 Elementary Educational Computer | 5-1 |
| 1. General structure of the Elementary Educational Computer (EEC) | 5-1 |
| 2. Presentation of the EEC units | 5-1 |
| 2.1. Memory Unit (MU) | 5-1 |
| 2.2. Arithmetic and Logic Unit (ALU) | 5-2 |
| 2.3. Control Unit (CU) | 5-3 |
| 2.4. Input/Output Units (I/O) | 5-4 |
| 3. The register structure of the EEC | 5-4 |
| 4. Mode of operation | 5-6 |
| 4.1. General considerations | 5-6 |
| 4.2. FETCH Phase | 5-6 |
| 4.3. EXECUTE Phase | 5-8 |
| A. Addition | 5-8 |
| B. Subtraction | 5-9 |
| C. Load | 5-11 |
| D. Store | 5-12 |
| E. Unconditional JUMP | 5-13 |
| F. Conditional JUMP | 5-14 |
| G. Input | 5-16 |
| H. Output | 5-17 |
| Chapter 6 Organisation of the CPU – peripheral devices communication | 6-1 |
| 1. Peripheral devices in the computer system | 6-1 |
| 2. Input/Output units | 6-2 |
| 3. Modes of transfer | 6-7 |
| 4. I/O processors (channels) | 6-8 |
| 5. Selector and multiplexer I/O processors (channels) | 6-11 |
| References | R-1 |
| Annex 1 CPU ORGANIZATION | |
| Annex 2 FETCH PHASE | |
| Annex 3 EXECUTE PHASE | |
| Annex 4 ALU WITH GENERAL REGISTER SET | |
| Annex 5 ELEMENTARY EDUCATIONAL COMPUTER | |
| Annex 6 TYPICAL I/O ARCHITECTURE | |